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APPLICATION NO.	. 1	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/810,034 03/26/2004		03/26/2004	Stephen M. Trimberger	X-1006-1D US	8432	
24309	7590	07/15/2005		EXAMINER		
XILINX, II			TAN, VIBOL			
ATTN: LEGAL DEPARTMENT 2100 LOGIC DR				ART UNIT	PAPER NUMBER	
SAN JOSE, CA 95124				2819		
				DATE MAILED: 07/15/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. 10/810,034 TRIMBERGER, STEPHEN M. TRIMBERGER, STEPHEN M. Examiner Whote Tan 2819 And unit 2819 As HORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MALINED DATE Of THIS COMMUNICATION. 1 Play barded for roly specified above is base han triefy (30) days, as reply with the studiety milerum of theiry (0) days will be considered finely. If the paried for roly specified above is base han triefy (30) days, as reply with the studiety milerum of theiry (0) days will be considered finely. If the paried for roly specified above is base han triefy (30) days, as reply with the start or demonstrated period for reply and triefy (30) days, as reply with the start or demonstrated period for reply and triefy (30) days, as reply with the start or demonstrated period for reply and triefy the start of the control of the provision of 37 (FR 1136(a)). In no event, however, may a reply be timely filled, and the start of the period for roly specified above is base ban triefy (30) days, as reply with the start or demonstrated period for reply the start of the provision of 37 (FR 1136(a)). In no event, however, may a reply be timely filled, and the control of the period of the provision of the provision of the provision of the main glate of this communication, even it timely filled, may reduce any seamed pearlier and alguments. Set of CFR 1.76(b). Status 1) Responsive to communication (s) filled on 26 March 2004. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-Z is/are pending in the application. 4) Claim(s) 1-Z is/are allowed. 5) Claim(s) 1-Z is/are allowed. 6) Claim(s) 1-Z is/are rejected. 7) Claim(s) 1-Z is/are rejected. 7) Claim(s) 1-Z is/are rejected. 8) The drawing(s) filed on 1/2 is/are start and the start and the start an	·			·
Examiner Vibol Tan 2819		Application No.	Applicant(s)	
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	Attachment(s)	·		
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)				•
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Notice of Draftsperson's Patent Drawing Review (PTO-948)	3) 🔯 Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) 🔲 Notice of Informal P)-152)

Application/Control Number: 10/810,034

Art Unit: 2819

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Young et al. (U. S. PAT. 5,963,050).

In claim 1, Young et al. teaches all claimed features in Fig. 6A, a method of propagating signals on interconnect in a programmable logic device, the method comprising: selecting (F5A between source signals (J, H) to drive a shared interconnect portion (a section from F5A to F6A&MH); and coordinating latching (RV, RZ) of the source signals at respective destinations (RV, RZ) with the selecting.

In claim 2, Young et al. further teaches the method of Claim 1 wherein the source signals are provided by a configurable logic block (100 in Fig. 1) in the programmable logic device.

In claim 3, Young et al. further teaches the method of Claim 1 wherein the source signals are provided by configurable logic blocks (plurality of logic block 100 of Fig. 1) in the programmable logic device.

In claim 4, Young et al. further teaches the method of Claim 1 wherein the destinations (RV, RZ) are provided in a configurable logic block (100 or tile) in the programmable logic device.

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In claim 5, Young et al. further teaches the method of Claim 1 wherein the destinations (RV, RZ) are provided in configurable logic blocks (100s or tiles) in the programmable logic device.

In claim 6, Young et al. further teaches the method of Claim 1 wherein the source signals include non-critical signals (inherent).

In claim 7, Young et al. further teaches the method of Claim 1 wherein the source signals include critical signals (inherent; col. 24, lines 39-48 explains about critical paths). Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN